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ANALYSIS AND DESIGN OF A SOFT-SWITCHING BOOST DC/DC CONVERTER

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***Abstract*:** This work investigates the analysis and design issues related to a boost DC/DC converter with soft switching. It provides a thorough explanation of the converter's working principles as well as a thorough examination of all of its operating modes.The suggested design enables zero-voltage switch activation by using a resonant circuit made up of two capacitors and an inductor. Along with providing a detailed description of the design concerns, the analysis also includes the computation of critical parameters for the resonant parts. This converter's ability to minimize voltage and switch losses is one of its notable advantages. Because of its soft-switching feature, this converter has the notable benefit of minimizing switching losses as well as the voltage and current strains on the circuit components. It also has a high switching frequency of operation. The advantages and disadvantages of this suggested structure are evaluated through a comparison with traditional topologies. Furthermore, the analysis validity is supported by simulation and experimental results using MATLAB software.

Keywords—Soft switching, step up converter, ZVS (zero voltage switching)

I. INTRODUCTION

DC/DC converters have many uses in the modern world in a variety of industries, including motor speed regulation, precision control instrumentation, aerospace, the military, and renewable energy interfaces [1-4]. These converters adjust a set DC input voltage to a variable output voltage in accordance with the needs of the load. They are placed between a DC voltage source and the load. Nevertheless, because of the strains that switching transitions in DC/DC converters place on the circuit components, energy losses frequently occur. As a result, designing converters with as little switching loss as possible is crucial. To attain this objective, it is imperative to guarantee that zero multiplies the output of the switch immediately prior to the transition [5-7]. Three main categories of approaches have been used to seek soft-switching, a highly desirable feature. Insulated gate bipolar transistors (IGBTs) are recommended in scenarios requiring ZCS conditions because their conduction loss is correlated with the average current rather than its peak value, leading to lower conduction losses. The resonant capacitor is an essential energy storage component in Cuk, SEPIC, and Zeta converters that needs a steady voltage. These designs however, come with significant current ripples. Certain topologies may experience high voltage pressures even when they use auxiliary components to provide soft-switching and lower component sizes and current stressors. ZVS transitions are incorporated into both the main and auxiliary switches in the topology, and a clamp diode is included to remove voltage oscillations. However, because of a higher freewheeling current, this method can decrease the ZVS range for both switches and increase conduction losses . High conduction losses may arise from the switch. Via a resonant circuit, another arrangement provides ZVS conditions; nevertheless, it necessitates intricate auxiliary circuits and high voltage strains.

II. SOFT SWITCHED BOOST CONVERTER

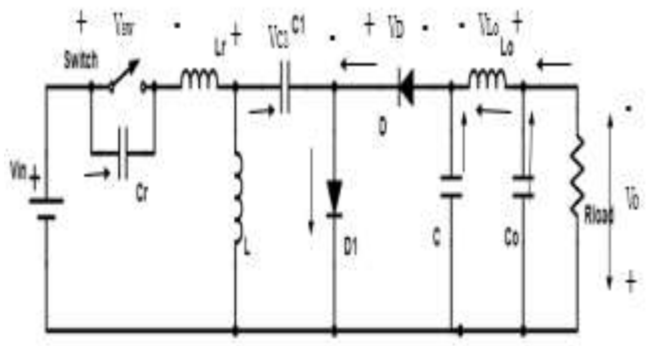

Fig. 1:*Circuit diagram of soft switched boost converter*

When the switch is turned on, this converter achieves zero-voltage switching (ZVS).when the switch is turned off capacitor connects source and load. The total of the clamping capacitor voltage and the load voltage determines the voltage stress on the switches. Nevertheless, this design incorporates a large number of energy storage components and semiconductor devices, which raises the losses of the circuit. ZVS is achieved by this design, while the switch is turned on. However, the large number of semiconductor parts and energy storage devices used in this arrangement result in higher complexity, higher losses, and higher costs. For soft-switching conditions, it has an additional active lossless snubber circuit. Like the earlier systems, this converter achieves ZVS during switch turn-on, reduces switching losses. This architecture has higher complexity, higher losses, and higher costs due to the large value of semiconductor devices and storage components. The technique presented in the paper involves using a resonant circuit and auxiliary parts to achieve ZVS conditions for the switches. The operational modes shows that during transitions, current and voltage stresses becomes low. There are thorough design considerations given. MATLAB software is used to confirm the theoretical analysis's accuracy with experimental and simulation data.

III. MODES OF OPERATION

Mode``1

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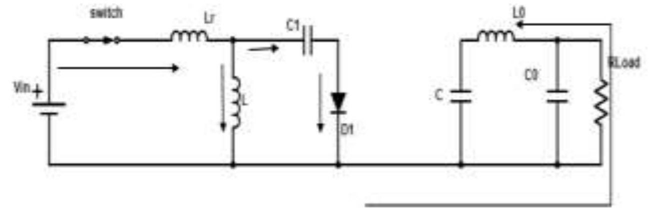

Fig 2: Circuit Diagram of Mode 1 of self-lift negative boost converter

In the mode 1 the switch operates and Diode D works as reverse bias where Diode D1 works in forward bias condition. The supply current flows through switch connects resonant inductance and capacitor C1 and Inductor L.As the diode D acts as reverse bias, load is not connected directly with the source.

The Voltage Across switch is zero, The switch current is equal to the supply current.

$$V_{sw} = 0 \tag{1}$$

$$I_{sw} = I_s \tag{2}$$

The Voltage across Diode D1 is zero .The current through the diode D1 is equal to the Current flows through the capacitor C1.

$$V_{D1} = 0 \tag{3}$$

$$I_{D1} = I_{C1} \tag{4}$$

The Voltage Across Diode D s maximum, Current through the diode D is zero.

$$I_D = 0 \tag{5}$$

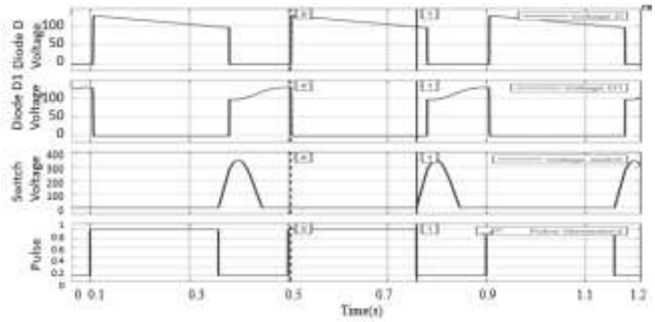

Fig 3: Voltage waveforms of Switch, Diode D and Diode D1 during mode 1 of converter

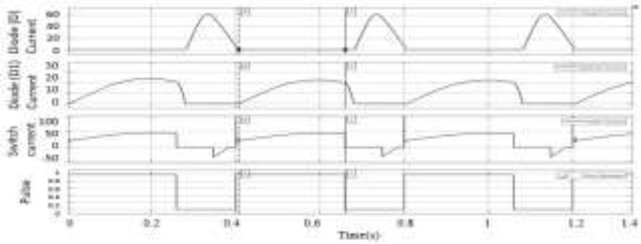

Fig 4: Current waveforms of Switch, Diode D and Diode D1 during mode 1 of the converter

Mode 2

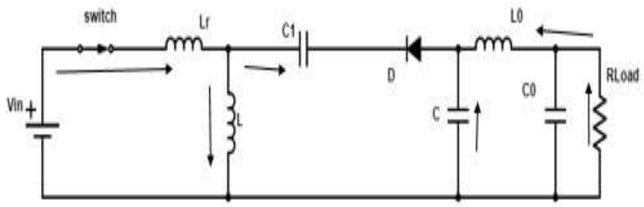

Fig 5: Circuit Diagram of mode 2 of self-lift negative boost converter

In the mode 2 switch turns on and connects the supply to the load, hence the supply current flows to the circuit through the switch and diode D. The Diode D acts as forward bias, The diode D1 acts as reverse bias.

The current through the switch is equal to the supply current, as the very minimum current flows through the resonant capacitor during switch turn on time The voltage across the switch is zero

$$I_{sw} = I_s \tag{6}$$

$$V_{sw} = 0 \tag{7}$$

The current through the diode D1 is zero, the voltage across the diode D1 is maximum.

$$I_{D1} = 0 \tag{8}$$

The Voltage across diode D is zero. The diode D current is equal to the summation of capacitor C current and Inductor Lo Current.

$$V_D = 0 \tag{9}$$

$$I_D = I_C + I_{Lo} \tag{10}$$

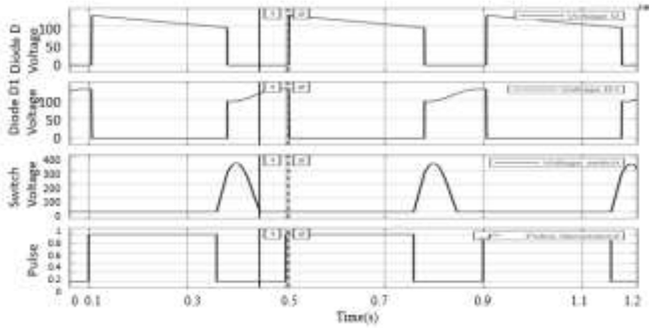

Fig 6: Voltage waveforms of Switch, Diode D and Diode D1 during mode 2 of converter

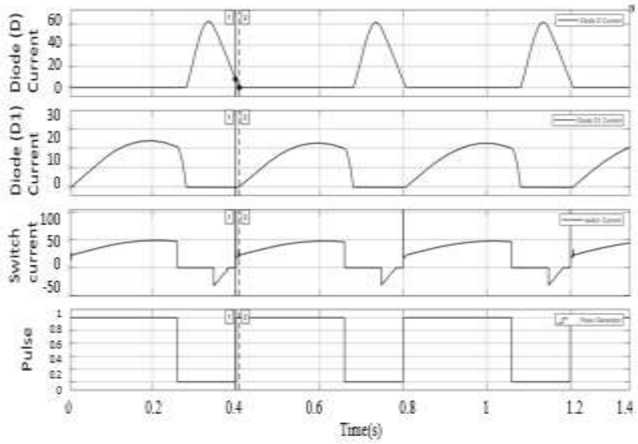

Fig 7: Current waveforms of Switch, Diode D and Diode D1 during mode 1 of the converter

Mode 3

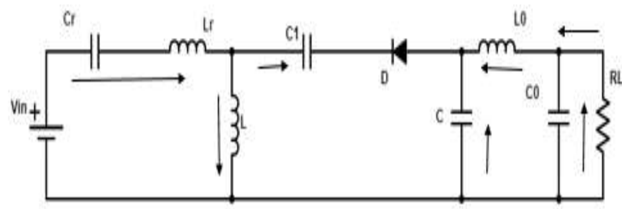

Fig 8: Circuit Diagram of mode 3 of self-lift negative boost converter

In the mode 3 switch turns off and disconnects from the supply, hence the supply current flows to the circuit through the resonant capacitor Cr. The Diode D acts as forward bias which connects source and load, The diode D1 acts as reverse bias. The switch voltage is maximum and switch current is zero.

$$I_{sw} = 0 \tag{11}$$

The diode D current is equal to the summation of capacitor C current and Load Current.

$$I_D = I_C + I_{Lo} \tag{12}$$

$$V_D = 0 \tag{13}$$

The diode D1 current is zero, and the voltage across the diode D1 is maximum

$$I_{D1} = 0 \tag{14}$$

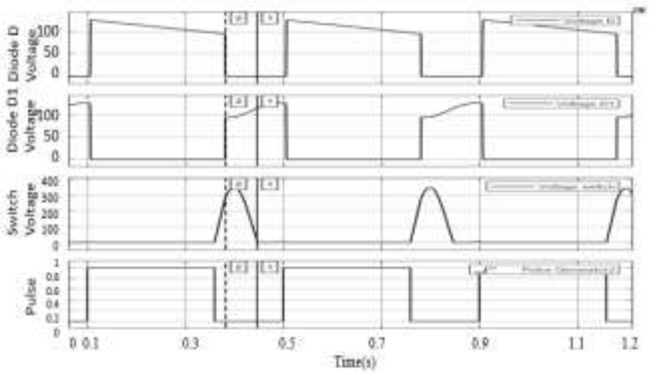

Fig 9: Voltage waveforms of Switch, Diode D and Diode D1 during mode 3 of converter

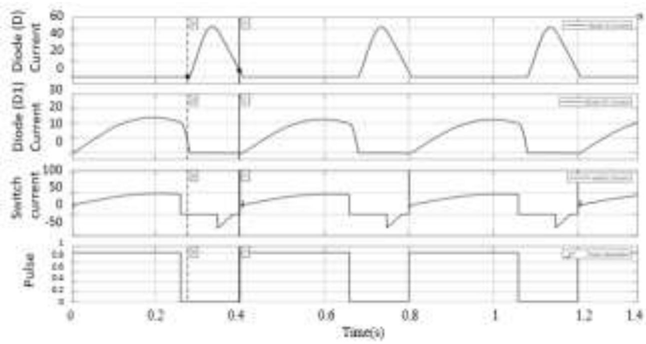

Fig 10: Current waveforms of Switch, Diode D and Diode D1 during mode 3 of the converter

Mode 4

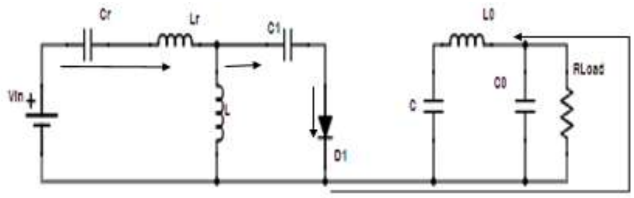

Fig 11: Circuit Diagram of mode 4 of self-lift negative boost converter

The mode 4 circuit diagram is shown in the figure where the switch continuous to be in off position. hence the supply current flows to the circuit through the resonant capacitor Cr. The diode D acts as reverse bias thus the source did not directly connected to the load. The diode D1 acts as forward bias thus one end of the capacitor C1 connects with the ground.

The switch current is zero, the voltage across the switch is maximum.

$$I_{sw} = 0 \tag{15}$$

The current through the diode D is zero and the voltage across the diode D is maximum.

$$I_D = 0 \tag{16}$$

The current flows through the diode D1 is equal to the capacitor current C1.

$$I_D = I_{C1} \tag{17}$$

The voltage across the diode D1 is zero.

$$V_{D1} = 0 \tag{18}$$

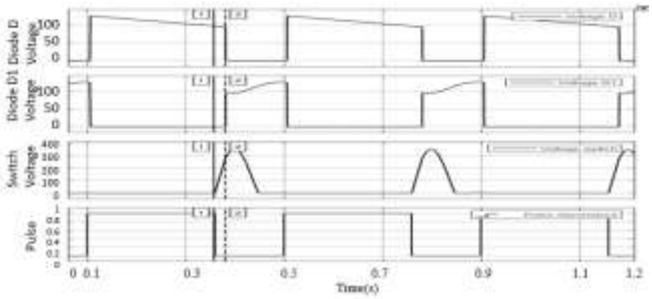

Fig 12: Voltage waveforms of Switch, Diode D and Diode D1 during mode 4 of converter

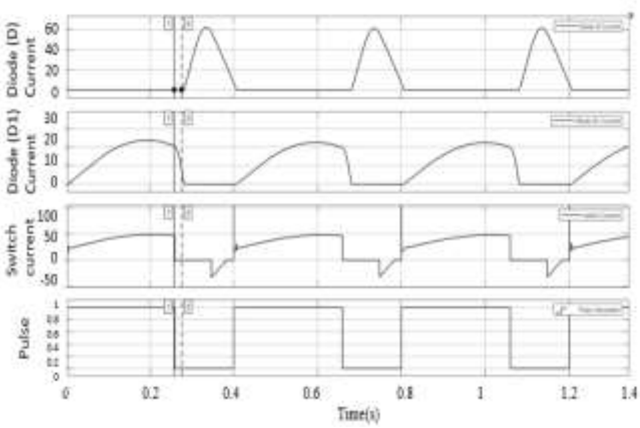

Fig 13: Current waveforms of Switch, Diode D and Diode D1 during mode 4 of the converter

IV. ANALYSIS AND SIMULATION RESULTS

The output voltage is given by

$$V_o = -V_{in}\frac{D}{1-D} \tag{19}$$

Where Vin represents Input Voltage.

D represents duty cycle

The duty cycle is given by ratio of time period required for the switch to be in on position (Ton) to the total time period (T)

$$D = \frac{T_{on}}{T} \tag{20}$$

When switch and diode 1 is in- on position and diode is in off position, source current is equal to resonant inductor current and sum of C1 current and L current.

$$I_s = I_{Lr} = (I_L + I_{C1}) \tag{21}$$

The source current is equal to resonant inductor current.

$I_s = I_{Lr}$ (22)

The source current is the splits to the inductor L and capacitor C1

$I_s = I_L + I_{C1}$ (23)

When the switch is continues to be in on position,diode1 off and diode conducts, load connects with the supply .when switch becomes off position and diode conducts and diode 1 becomes reverse biased .load directly connects with the supply.

$I_{sw} = I_s$ (24)

The Inductance L Current is equal to the summation of source current and diode current D.

$I_L = I_s + I_D$ (25)

The resonant inductor current is equal to the source current.

$I_{Lr} = I_s$ (26)

When the switch turns off ,diode continuous to be in forward biased position ,diode 1 is in reverse biased condition. The supply flows to the circuit through resonant capacitor Cr.

$I_{cr} = I_s$ (27)

The source current is equal to the resonant Inductance Lr current.

$I_s = I_{Lr} = I_{Cr}$ (28)

The Inductance L Current is equal to the summation of source current and diode current D.

$I_L = I_s + I_D$ (29)

When the switch continues to be in off position diode becomes reverse bias and diode 1 is forward bias and conducts. capacitor C and inductor Lo discharges and supplies current to the load.

$I_{Lo} = I_o$ (30)

The resonant inductor Lr current is equal to the supply current.

$I_s = I_{Lr}$ (31)

The supply current splits into two parts and flows to the inductance L and Capacitor C1.

$I_s = I_L + I_{C1}$ (32)

The simulation is done using MATLAB Simulink software where the results of resonant parameters and output voltage and current were taken as waveforms. The simulation diagram is shown in the figure 2. The figure 3 represents the load current and load voltage and the figure 4 shows the resonant parameters

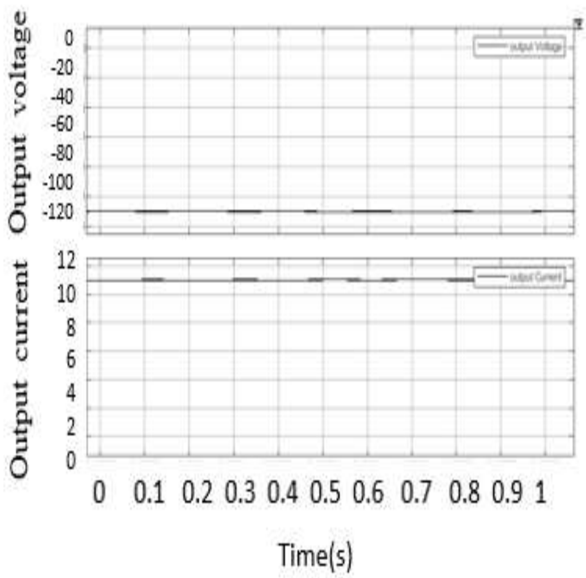

Fig 14: Load voltage and Load current

The source voltage is given as 48V and the resulted load voltage is - 110V. negative indicates as negative boost converter.

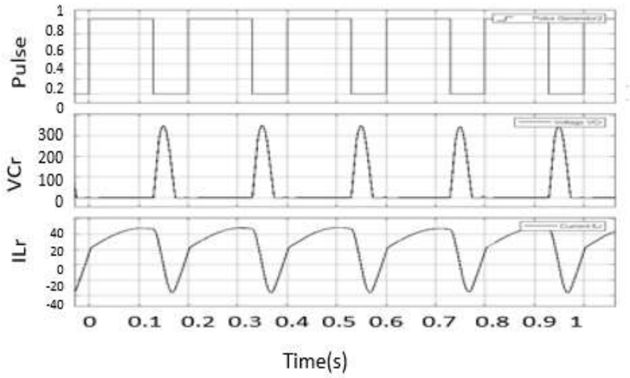

Fig 15:Resonant Inductor and Capacitor with respect to pulse

When the switch conducts the capacitor voltage becomes high and when switch is in off position capacitor voltage will be low. when switch conducts inductor charges and discharges when capacitor connects.

V. CONCLUSION

In this study, a soft-switching boost DC/DC converter is analyzed, designed, and its experimental and simulation results are presented. The goal of implementing the soft-switching technology is to reduce the system's internal voltage and current stressors. Interestingly, the voltage between the switches drops to zero at the end, enabling both switches to initiate zero-voltage switching (ZVS) .Moreover, because the currents in both switches climb gradually after the ON transition, they undergo very little stress. It is noteworthy, nevertheless, that because there are no zero-current switching (ZCS) conditions present, both switches experience hard switching during the turn-off transitions. Equations obtained throughout the study. The ratio is crucial when choosing between inductors and capacitors. Seven criteria are used in a thorough assessment to compare the suggested structure to conventional topologies. The suggested configuration reduces the voltage and current strains on the primary and secondary switches and provides ZVS conditions during ON transitions.

REFERENCES

[1]. Ebrahim Babaei1,2 , Amin Abbasnezhad1, Mehran Sabahi2, Seyed Hossein Hosseini1” Analysis and design of a soft-switching boost DC/DC converter”, IET Power Electron., 2017, Vol. 10 Iss. 11, pp. 1353-1362

[2]. Senthilkumar, R. and Uma, G. “Design of ZVS Voltage Boost DC-DC Converter”, Wulfenia Journal, Austria, ISSN: 1561-882X, Vol.19, No.11, pp.334 -345, November 2012.

[3]. Y. Li, Y. Wang, H. Song and D. Xu, "Analysis and Design of a Nonisolated Bidirectional DC–DC Converter Based on CLC Network," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 2, no. 4, pp. 481-490, Oct. 2021, doi: 10.1109/JESTIE.2021.3096731

[4]. Luo, Fang Lin, and Hong Ye,“ Advanced DC/DC Converters”, CRC Press,2004

[5]. P. Channegowda, P. Rengasamy, D. Ludois and G. Venkataramanan, "High Voltage DC- DC Converter Topology based on Capacitive Coupling with Soft Switching Characteristics," 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, 2020, pp. 1-6

[6]. I.-D. Kim, J.-Y. Kim, E.-C. Nho, and H.-G. Kim, “Analysis and Design of a Soft-Switched PWM Sepic DC-DC Converter,” Journal of Power Electronics, vol. 10, no. 5. The Korean Institute of Power Electronics, pp. 461–467, 20-Sep-2010

[7]. Podila Purna Chandra Rao, Radhakrishnan Anandhakumar, L. Shanmukha Rao," Analysis of a novel soft switching bidirectional DC-DC converter for electric vehicle", Bulletin of Electrical Engineering and Informatics (BEEI),Vol.12. no.5.pp.4505,2011

[8]. Amir Ostadi, Xing Gao and Gerry Moschopoulos, "Circuit Properties of Zero-Voltage-Transition PWM Converters ", Journal of Power Electronics, Vol. 8, No. 1, January 2008

[9]. Rashid M. H, "Power Electronics handbook: devices, circuits, and applications". Academic Press, 2007.

[10]. Mohan N., TM. Undeland, W.P. Robbins. "Power Electronics - Converters, Applications, and Design (3rd Edition)", John Wiley & Sons, 2003.